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An experimental simple digital field-store synchroniser for system I television

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AN EXPERIMENTAL SIMPLE DIGITAL FIELD-STORE SYNCHRONISER FOR SYSTEM I TELEVISION

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Summary

Synchronisation of television picture sources is a necessary prerequisite for modern programme production methods. Within a studio centre, this is normally achieved by permanently arranging the timings of the signals within the centre to be synchronous. However, this method is not possible for peripatetic remote sources such as outside broadcast units and very difficult even for fixed remote sources.

Two methods are available which can synchronise such sources, at least to within an acceptable error range. The first, used in the BBC 'Natlock' system, relies on a comparison of the timings of the remote source and the reference to generate an error signal which can be used to alter the timing of either the source or the reference in such a way as to reduce the error to an acceptable value. The second method uses a variable delay, usually in the source signal chain, to alter the relative timing between source and reference. This variable delay and its associated (automatic) controls are usually referred to by the collective title of 'a field (or picture or frame)-store synchroniser'.

Potential applications in the BBC for a new, relatively inexpensive field-store synchroniser are considered, and the basic requirements of such a device are identified. As a result of recent developments in methods of storing digital video signals, it is now feasible to provide simple, digital 'full-range' synchronisers in relatively large numbers. These could be used to achieve complete network synchronism and replace the Natlock equipment currently in use.

The design philosophy and circuit details and the problems which would be encountered in the design of a production synchroniser were investigated using an experimental prototype based on an existing digital picture store.

The experimental results showed that apart from a number of difficulties and restrictions mainly incurred by not having a store specifically designed for use in a synchroniser, the basic ideas and most of the final circuit arrangements were adequate.

Issued under the authority of

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AN EXPERIMENTAL SIMPLE DIGITAL FIELD-STORE SYNCHRONISER FOR SYSTEM I TELEVISION

R. Walker, B.Sc.(Eng.)

1. Introduction

Picture source synchronisation within the BBC television service is presently achieved mainly by the use of 'Natlock' correction equipment. This method achieves synchronism of two picture sources at a specified point by feeding timing correction signals from a comparator at that 'mixing point' to either the local or the remote pulse generators. Usually, the local pulse generator is left undisturbed and the corrections are applied to each of the remote sources individually. This method requires one complete set of comparison equipment and one return control-channel (telephone quality) for each of the remote sources. It also requires, at each remote source, a pulse generator which is capable of accepting these correction signals, after they have been decoded. One disadvantage of the Natlock system is the long lock-up time (6 minutes maximum), which means that to achieve synchronous cutting or mixing between the sources, the 'new' signal must be available for that length of time before being selected on the vision mixer. This is not normally a serious disadvantage as such things can be pre-planned. However, for some current affairs and sports programmes, changes to the running schedule during the programme are made more difficult because of the lack of the necessary time to change the synchronising arrangements.

In addition, there is no way in which this technique, used alone, can make two signals synchronous with each other in two different places at the same time.

An alternative way of achieving synchronism is by introducing a delay into the signal path. This delay must be varied automatically, depending on the difference in timing between the input signal and the output reference. To be generally applicable, synchronisers of this type must be 'full-range', that is, capable of correcting any difference in timing between input and output and this requires at least one field of storage or delay. Within the last few years, developments in methods of storing digital signals have made it possible to store whole fields for long periods of time for quite a small capital outlay. Moreover, these stores can be designed to work fast enough to process the signal in 'real time'. It is now therefore reasonable to consider providing simple synchronisers in relatively large numbers as a studio facility, rather than in small numbers as a centralised facility, as they are at present.

The requirements emerging for new picture source synchronisers within the BBC can be divided into two general categories. The first is for a general-purpose machine with a number of facilities, such as an ability to produce frozen or reduced size pictures and the capability of handling non-mathematical* PAL signals. This will be complicated and fairly expensive. The second is for a simple machine, whose function will be solely network synchronisation of mathematically correct PAL video signals, wholly or partly to replace the present Natlock methods. It will have wide application and must, therefore, be as cheap as possible. This simpler, cheaper option, using only one field of storage, is the subject of this present work and is the only one considered in the remainder of this report. Experiments have been carried out, using the Research Department picture store completed in 1975,[1] culminating in an experimental simple synchroniser. These experiments were done to identify the problems which would be encountered in the design and construction of such a machine and to evaluate their possible solutions.

2. The basic requirements for a simple synchroniser and performance targets

Fig. 1 shows a block diagram of a basic digital synchroniser.

2.1. Range

The main basic requirement of a simple synchroniser is that it should be full-range, that is, it must be able to accept any input-picture timing relative to the output reference and produce a stable output, synchronised with the local reference, preferably with a manually variable offset of limited range, to allow compensation for different cable lengths and alternative connections within its immediate environment.

2.2. Picture quality

No continuous picture degradations should be introduced in addition to those inevitably associated with the sampling and quantisation of the signal during normal** operations. This requirement means that the signal must be processed as a composite video waveform without being decoded into separate luminance and chrominance components.

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* Mathematical PAL is a composite video waveform in which the relationship between the colour subcarrier frequency, f_{SC}, the line frequency, f_L, and the field frequency, f_F, is exactly as defined in the PAL specification, that is: $f_{SC} = 1135.f_L/4 + f_F/2$ Hz, and $f_L = 625\ f_F/2$. With such relationships, there is an integral number of subcarrier periods in eight field periods.

** Normal is defined as the operation with undisturbed input and reference signals.

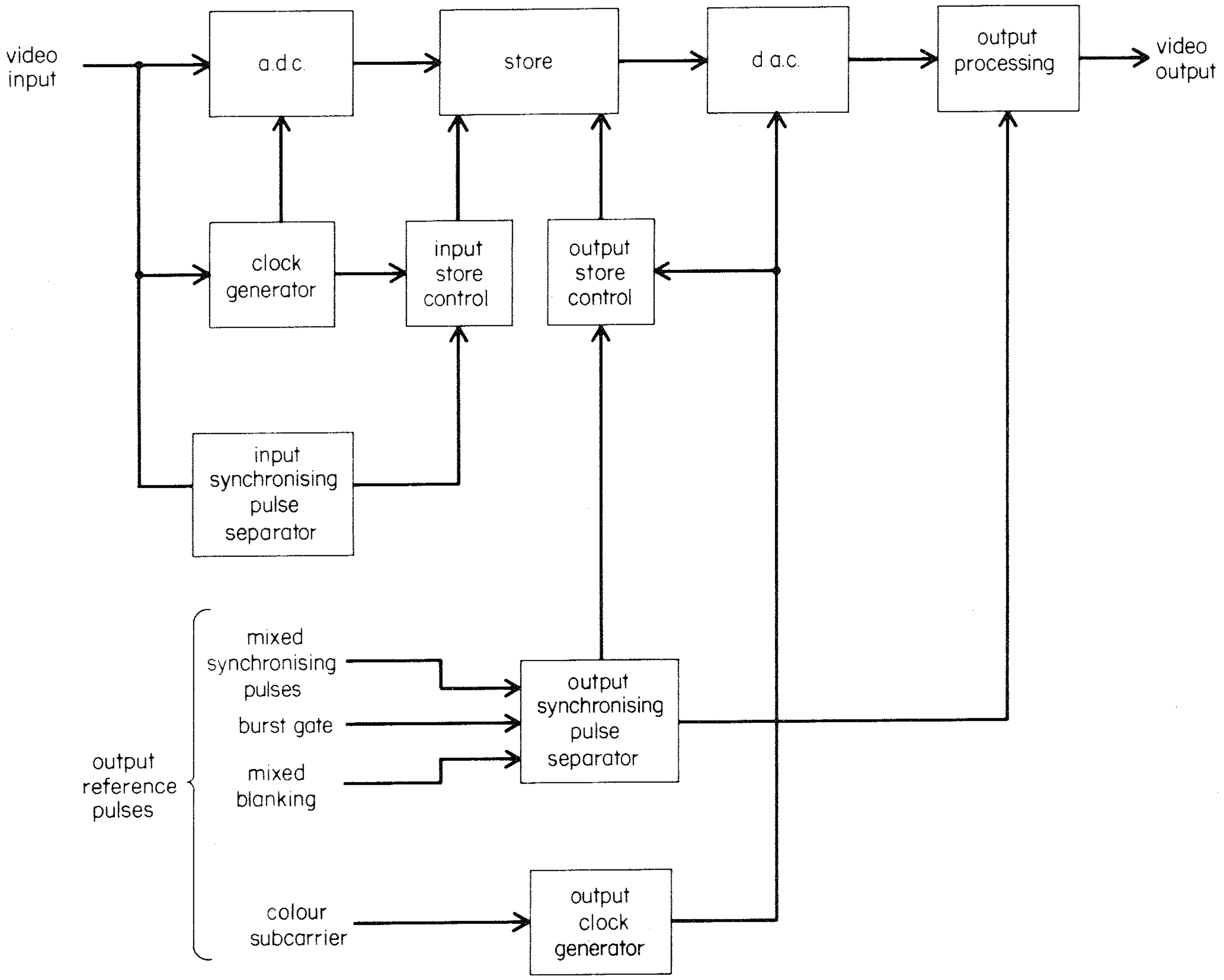

Fig. 1 - Block diagram of a basic digital synchroniser

2.3. Non-synchronous cuts

Non-synchronous cuts in the input must not produce any unacceptable effects* in the output picture and must not disturb the output synchronising pulses and colour burst.

2.4. Non-mathematical inputs

The normal input would be mathematically correct PAL or monochrome waveforms, but inputs which have been subject to continuous 'colour-rate' or 'slow-rate' Natlock corrections (±1 ns and ±18 ns per picture respectively) should not unduly disturb the output. Intermittent colour corrections allowed in a locked Natlock system should have no perceptible effect. It is also preferable that a recognisable output be produced from inputs which have been subjected to 'fast-rate' corrections (±180 μs per second) or line dropping/adding corrections (2 lines per field with Natlock).

2.5. Output stability

The output should be as stable as possible, certainly to within $\pm 2^\circ$ of colour subcarrier phase. Any residual jitter should be confined to very low frequencies of modulation of the output signal timing.

2.6. Lock-up time

The total lock-up time after a non-synchronous cut should be as short as possible. The theoretical minimum for the worst-case lock-up time is 2 field periods. For practical reasons, it would be difficult to do better than 2½ field periods, worst-case.

The output picture during the lock-up time can only be derived from information stored just before the cut. With only one field of storage, this output will be made up from parts of two input fields.

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* During the lock-up time of the input circuits, some form of picture degradation is inevitable. This is likely to be a 'frozen' field or picture, made up from information held in the store at the time the cut is detected and will be of limited duration, normally 1–2 fields (see Section 2.6).

2.7. Vertical interval signals

In the normal location envisaged for synchronisers that is, prior to mixers, there is no requirement for the Vertical Interval Test Signals or CEEFAX to be transferred from the input to the output. In special applications, it may be necessary to process these parts of the video waveform separately by stripping them off the input prior to synchronisation and re-inserting them afterwards.

3. Design considerations

3.1. Store size

The minimum amount of storage required for a full-range synchroniser is that necessary to store the data representing one active field. At $3f_{sc}$ sampling frequency, the active line length is approximately 692 samples long and the active field consists of 287½ lines. This is equal to 198,950 samples of 8 bits each, or approximately 1·59 Mbit. In practice, allowance has to be made for tolerances and end-effects (see Section 5.5).

The usual binary arrangement of commercial storage devices means that the smallest practicable storage array with adequate speed and word length has a capacity of 2·097 Mbit, considerably larger than the theoretical requirement.

3.2. The 8-field sequence

The 625-line television synchronising pulses divide the picture into 2 interlaced fields, usually called 'even' and 'odd' fields. The PAL colour system, in which the phase of the V component of the chrominance, or V-axis, is inverted on alternate lines, further divides up the field-sequence, giving a total of 4 different kinds of field.

These can be defined as follows:

Field type 1: even, V-axis non-inverted on odd numbered lines

TABLE 1

OUTPUT FIELDS		INPUT FIELDS							
		4A	1A	2A	3A	4B	1B	2B	3B
4A		N	N−313	N+1	N−312	N	N−313	N+1	N−312
	V	0	−½	+1	+½	0	−½	+1	+½
	H	0	180	180	0	180	0	0	180
1A		N+313	N	N+312	N+1	N+313	N	N+312	N+1
	V	+½	0	−½	+1	+½	0	−½	+1
	H	180	0	180	180	0	180	0	0
2A		N+1	N−312	N	N−313	N+1	N−312	N	N−313
	V	+1	+½	0	−½	+1	+½	0	−½
	H	0	180	0	180	180	0	180	0
3A		N+312	N+1	N+313	N	N+312	N+1	N+313	N
	V	−½	+1	+½	0	−½	+1	+½	0
	H	0	0	180	0	180	180	0	180
4B		N	N−313	N+1	N−312	N	N−313	N+1	N−312
	V	0	−½	+1	+½	0	−½	+1	+½
	H	180	0	0	180	0	180	180	0
1B		N+313	N	N+312	N+1	N+313	N	N+312	N+1
	V	+½	0	−½	+1	+½	0	−½	+1
	H	0	180	0	0	180	0	180	180
2B		N+1	N−312	N	N−313	N+1	N−312	N	N−313
	V	+1	+½	0	−½	+1	+½	0	−½
	H	180	0	180	0	0	180	0	180
3B		N+312	N+1	N+313	N	N+312	N+1	N+313	N
	V	−½	+1	+½	0	−½	+1	+½	0
	H	180	180	0	180	0	0	180	0

For line N of output read line shown of input field. V (in field-line spacing) and H (in degrees of colour subcarrier phase) give vertical and horizontal output picture position errors. (N lies between 1 and 312½ for Fields 1 and 3 and between 312½ and 625 for Fields 2 and 4).

Field type 2: odd, V-axis non-inverted on odd numbered lines
Field type 3: even, V-axis non-inverted on even numbered lines
Field type 4: odd, V-axis non-inverted on even numbered lines

The line numbering and definitions of odd and even fields are conventional, and are as described in Reference 2.

One group of four such fields is followed by a second group of four fields defined in the same way, but with the phase of the colour subcarrier shifted by 180°. This Sequence of 8-fields is repeated continuously as the relationship between colour subcarrier frequency and the line frequency is such that an integral number of subcarrier cycles is contained in the 8-field periods.

For a non-decoding synchroniser with less than 8 fields of storage, the implication of this sequence is that any type of input field may have to be converted into any other type of field at the output. This can always be done by shifting the picture information at the output away from its true position relative to the output synchronising pulses, so that the phases of the V-axis switch and colour subcarrier are compatible with the output reference.

The horizontal shift may be up to ½ subcarrier period (approximately 113 ns) in either direction and, with a single field store, the vertical shift may be 1 field-line up or down. Table 1* gives all of the possible combinations of input and output fields, together with the line-store addressing modifications and the resulting vertical shift of the picture in field lines. The fields in Table 1 have been divided into two groups of 4, labelled A and B respectively. Field 4 is shown first in order to conform with the notation of Ref. 2. The horizontal shifts are given only as 0° and 180° relative to an arbitrary reference, as the colour subcarrier phase, relative to the 8 field sequence, is not defined and so the absolute horizontal shift of the picture cannot be specified.

During normal operation, the locus followed is a diagonal progression at 45° downwards and from left to right. It can be seen from Table 1 that any such diagonal passes through positions of equal picture shift,** thus showing that the shift is constant and gives a stable output picture for any phase of input relative to output. If the phase of the input relative to the output goes beyond the point where the store either fills up or becomes empty, then the store programme must jump to an adjacent diagonal. Such a jump will always be accompanied by a sudden movement of the output picture vertically but not always horizontally. Hysteresis must therefore be incorporated in the decision circuits to avoid jumping continuously between two diagonals when the input and output are nearly synchronous.

Table 1 and therefore the control logic can be simplified if the lines of odd and even fields are both labelled from 1 to 313 in such a way that a line labelled L is related to a line number N by L=N for even fields (N<313) and L=N−312 for odd fields (N⩾313). In addition, for consideration of the vertical picture shifts, the 8-field sequence can be reduced to a 4-field sequence, as the second group of 4 fields is identical to the first, the only difference being one of 180° of the colour subcarrier. Table 1 can now be modified to give Table 2. In the store, this label is used as the storage address. The arithmetic then simply consists of either adding to or subtracting one from the read address, as and if required.

TABLE 2

			INPUT FIELDS			
			4	1	2	3
OUTPUT FIELDS	4		L	L−1	L+1	L
		V	0	−½	+1	+½
		H	0	180	180	0
	1		L+1	L	L	L+1
		V	+½	0	−½	+1
		H	180	0	180	180
	2		L+1	L	L	L−1
		V	+1	+½	0	−½
		H	0	180	0	180
	3		L	L+1	L+1	L
		V	−½	+1	+½	0
		H	0	0	180	0

For line N of output field convert N to label number L and read out line with label given in Table. *V* and *H* give vertical and horizontal output picture position errors. (L = N for N<313, L = N−312 for N⩾313).

3.3. Choice of clock frequency

A fundamental consideration was the choice of sampling frequency, i.e. clock frequency, as this affected the detail design of a considerable fraction of the experimental prototype. The clock frequency must be locked to the video synchronising signals in a known way or the precise delay through the store becomes indeterminate. The choice lay between a clock frequency which was an integral multiple of the television line frequency and one which was a simple multiple of the colour subcarrier frequency. In addition, the clock frequency had to be high enough to describe the video signal adequately, yet not so high that the amount of storage required was excessive. In practice, the choice lay between $851f_L$ and $3f_{sc}$. Both of these are approximately 13·3 MHz, which is sufficiently above the theoretical (Nyquist) minimum of 11·0 MHz to make the input and output filters easy to construct.

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* Orignally devised by M.G. Croll

** The address sequences like N−313, alternating with N+312, which occur on every other diagonal, correspond to a constant shift where an odd field is being changed into an even field or vice versa.

Other work has shown that $3f_{sc}$ sampling gives very slightly less picture degradation. However, the experimental prototype was first designed and constructed using $851f_L$ sampling as this simplified the control logic. To obtain the correct colour lock with this sampling structure, a phase comparator was required at the output of the synchroniser to control the phase of the output clock. This compared the phase of the colour subcarrier burst coming through the store with the local reference subcarrier and generated an error signal to control the output clock generator in such a way as to minimise the error. It was found, however, that this comparator was unable adequately to remove the output jitter caused by the inherent timing instability of the line-locked clocks. Also, this comparator introduced an inevitable and sometimes objectionable delay before the new output was correctly phased

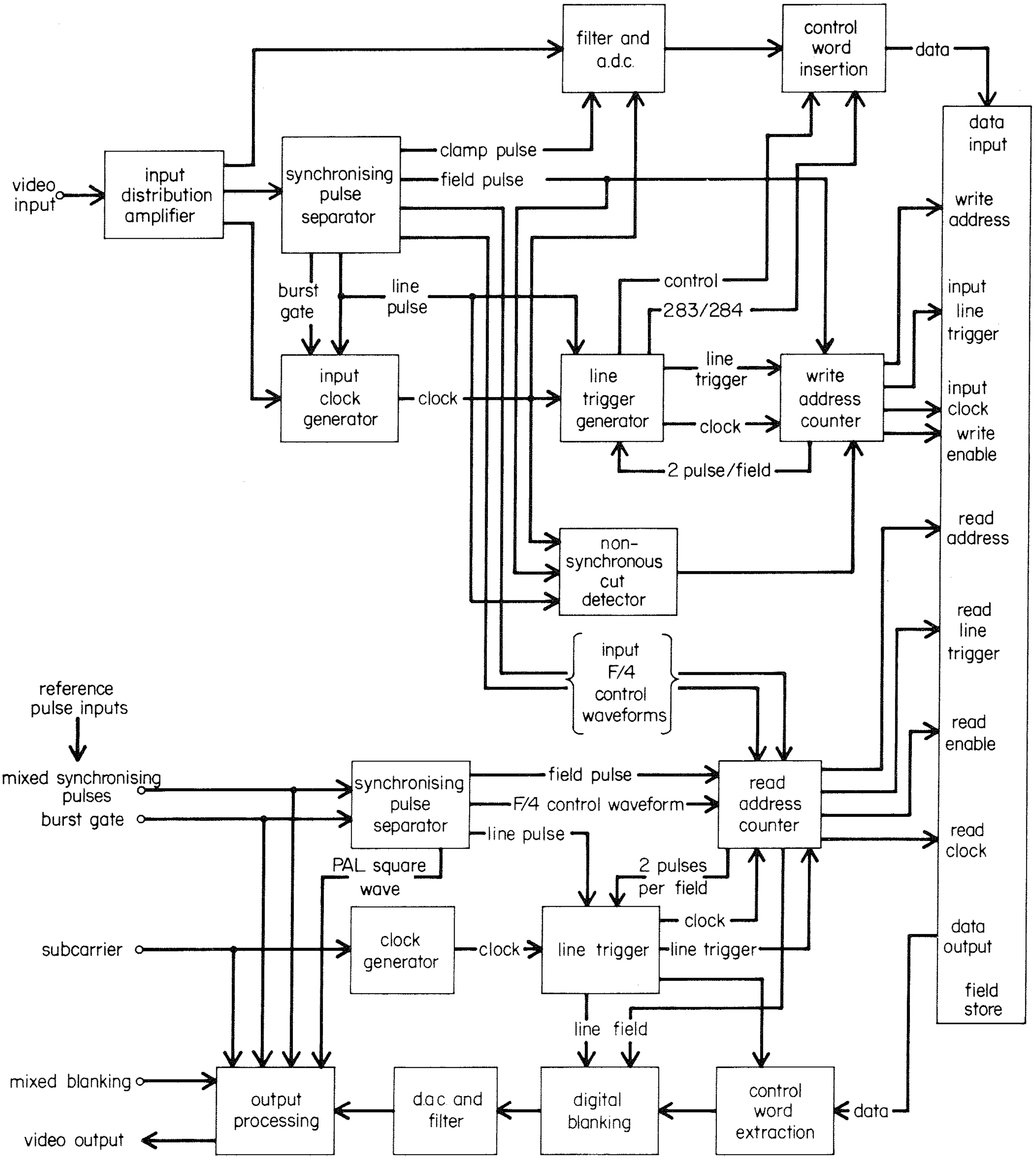

Fig. 2 - Block diagram of the experimental prototype simple full range digital synchroniser

after a non-synchronous cut. Accordingly, the experimental prototype was modified to use $3f_{sc}$ clocks. This choice, however, makes the store control logic more complicated and the processing of monochrome signals somewhat more difficult.

These points are more thoroughly discussed in Section 5 and in Appendix 2.

4. The experimental simple synchroniser

Fig. 2 shows a block diagram of a simple, full-range, digital synchroniser, in the final form of the experimental prototype.

4.1. Synchronising pulse separators

The input synchronising pulse separator was based on

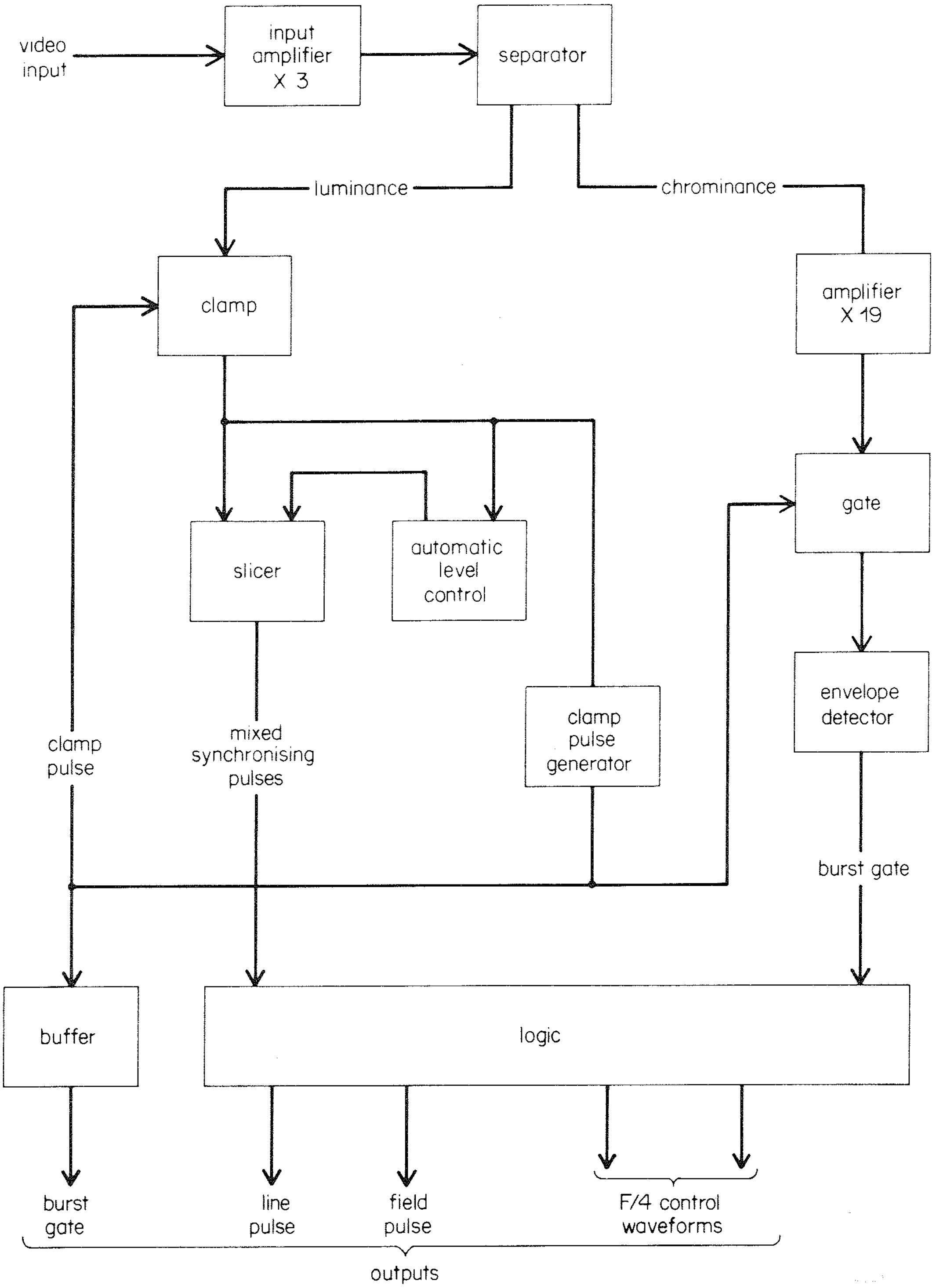

Fig. 3 - Block diagram of the input synchronising pulse separator

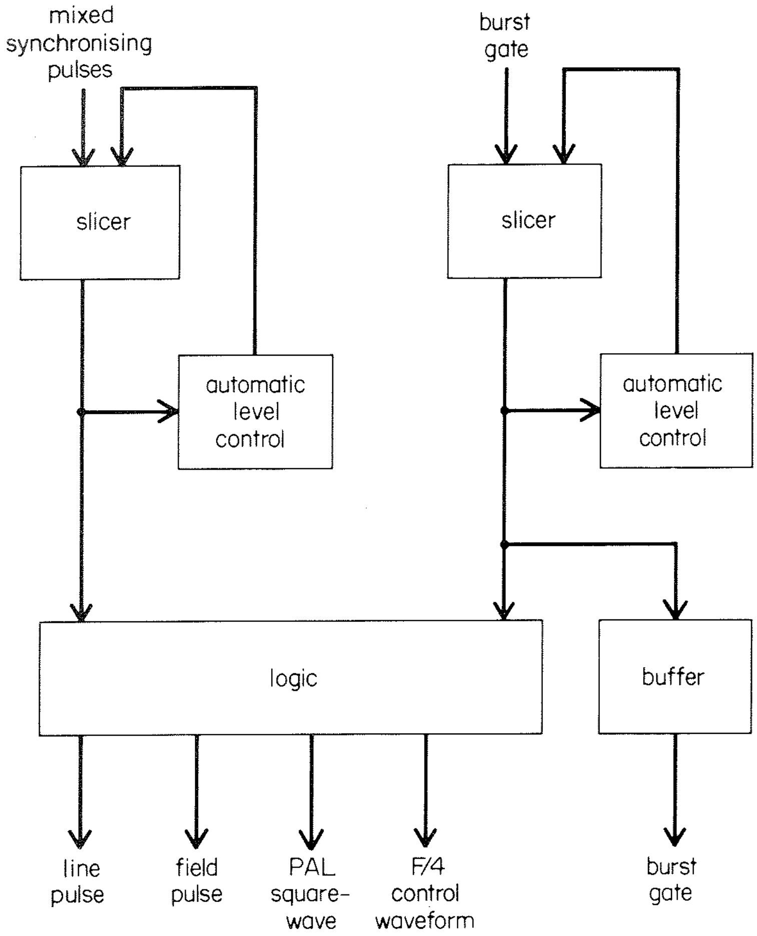

Fig. 4 - Block diagram of the output synchronising pulse separator

a conventional analogue design. Fig. 3 shows an outline block diagram of it. After the chrominance information has been filtered out, the clamped video waveform was applied to a slicing circuit. The slicing level was automatically maintained at a level equivalent to halfway down the synchronising pulses, in order to compensate for variations in input level. The resulting synchronising pulse waveform from the slicer was processed by the logic circuit to separate line pulses, field pulses, burst gate and two 'F/4' waveforms, each at one-quarter of the field-rate, which together defined the input 4-field sequence. A clamp pulse is also produced for use within the separator. The chrominance information was used to drive a burst detector, the output of which, utilizing the fact that the first burst of a new field is always on a line with a positive sense of V-axis switch, was used to check the phase of the bistable device which produced PAL square-wave. This was used internally to derive one of the quarter field-rate waveforms.

The output synchronising pulse separator was similar in principle to the input separator, but it was somewhat simpler because it was supplied with synchronising pulses instead of video signals. In particular, there was no luminance/chrominance separation stage and the automatic variation of slicing level was less complex. Fig. 4 shows a block diagram. It required inputs of mixed synchronising pulses and burst gate pulses and gave outputs of line pulses, field pulses, burst gate, PAL square-wave and a single one-quarter field-rate waveform to define the phase of the output 4-field sequence.

4.2. Clock oscillators

The input clock generator was a conventional type of phase detector which compared the phase of the chrominance of the input signal with that of the input clock divided by 3. The phase detector output was sampled at a time corresponding to the location of the subcarrier burst and the resulting voltage, suitably amplified and filtered, was used to control the frequency and phase of the input clock oscillator. A block diagram of the input clock oscillator system is given in Fig. 5.

A compromise has to be made, for this application, between the loop noise bandwidth and the lock-up time and pull-in range. The value finally chosen for the damped natural frequency was 200 radian.s^{-1} and a damping coefficient of 0·77. This gave an effective noise bandwidth of about 60 Hz, a maximum pull-in time for a random jump of input phase of 60 ms (90% confidence limit) and a pull-in range of about 30–40 Hz at the subcarrier frequency.

This performance was barely adequate, particularly in pull-in time, so a different kind of loop would probably have to be used. This point is discussed more thoroughly in Section 5.2.

The oscillator ($3f_{sc}$) output was used directly to drive the analogue to digital converter and the circuits handling video data, including the store. Most of the remainder of the logic, that is, the store control logic was clocked at f_{sc} by output of the $\div 3$ circuit, which was

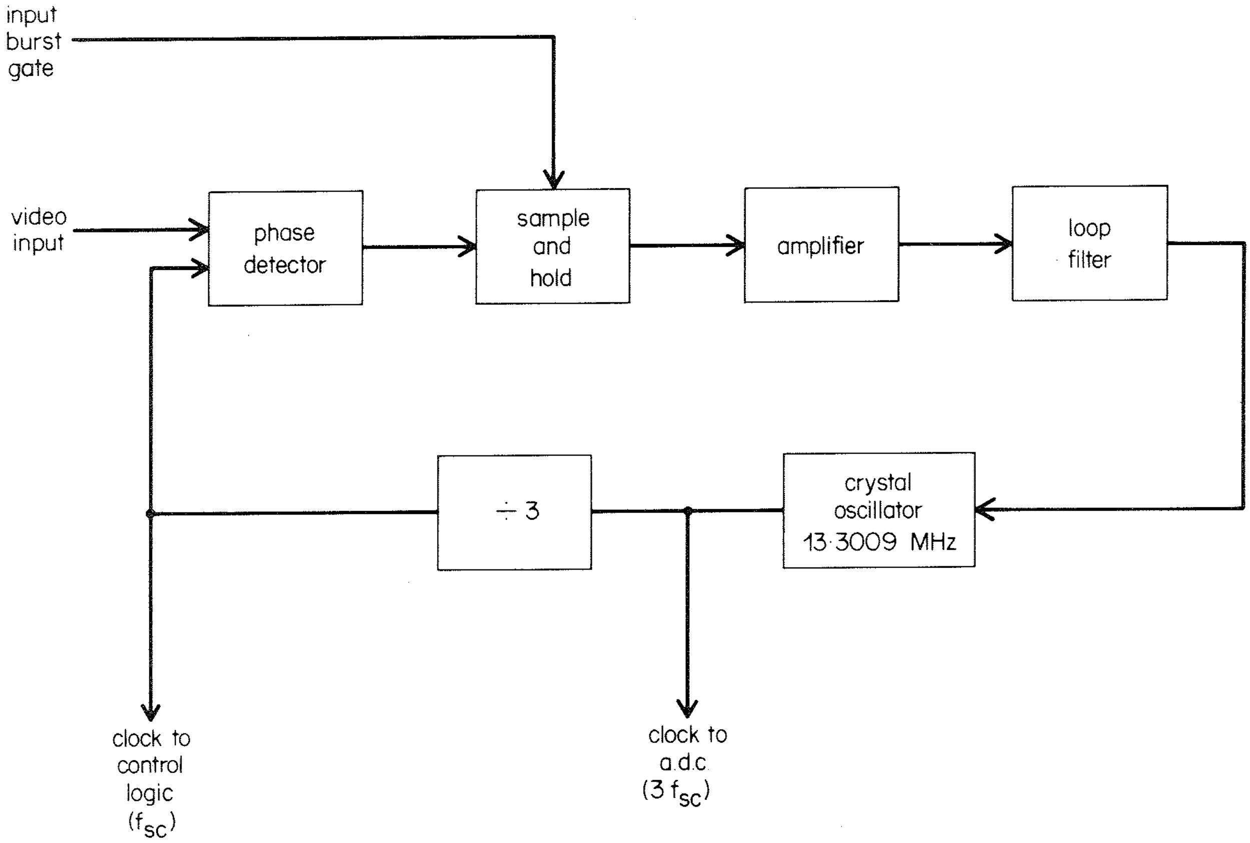
input burst gate
video input
phase detector
sample and hold
amplifier
loop filter
÷ 3
crystal oscillator 13·3009 MHz
clock to control logic (f_{sc})
clock to a.d.c ($3f_{sc}$)

Fig. 5 - Block diagram of the input clock system

directly locked to the input subcarrier. In this way, all of the control logic was operated at subcarrier rate thus easing the logic design and, more importantly, ensuring that the colour phasing at the output was automatically achieved, given that the output circuits operated in a similar manner. Without this, some other method of eliminating the one-of-three ambiguity of the colour phase would have been needed.

The output clock generator was considerably less complicated than the input as it was locked to a continuous feed of reference subcarrier and there was no requirement for a rapid acquisition of a new signal. Two options were feasible, one was to use a simple phase-lock loop with a divide-by-3 circuit as in the input loop and the other was to use a simple analogue x3 multiplier and slicer. The option chosen was the phase-lock loop because it would be less liable to drift in phase than would the relatively high selectivity filter required by the multiplier.

The final parameters of this loop were the same as for the input loop, a damped natural frequency of 200 radian.s^{-1} and a damping coefficient of 0·77.

4.3. Line trigger generators

For economy, only about 58 μs from each 64 μs line-period was stored. A pulse had to be derived from the input signal to define the start of this active line period and initiate the storage of data for each line period. Similarly, at the output, a pulse had to be derived from the reference signal to initiate the output of data from the store. These two pulses, called input and output line trigger pulses respectively, had to be obtained from the clock and line pulse waveforms, and had to be positioned accurately relative to the line synchronising pulse edges. The circuits to do this were virtually identical, so only the input circuit is considered in detail.

With line-locked clocks, this operation was almost trivial as the waveforms are line repetitive; the clocks were merely divided by the appropriate number (851) and a phasing circuit ensured that the divider output occurred in the position required to provide the correct timing of line triggers.

With subcarrier locked clocks, however, the waveforms are not line repetitive. The division ratio had therefore to be continuously changed according to some predetermined sequence in order to keep the line trigger pulse in the correct mean position relative to line synchronising pulses. Thus, the part of the line which was stored was continuously changing about some mean position. A block diagram of the circuitry used to generate line trigger pulses with a $3f_{sc}$ sampling frequency is shown in Fig. 6. Its operation may be explained as follows.

After 8 field periods the phase of the colour subcarrier relative to the synchronising pulses repeats and so the division ratio sequence had to be such that it was

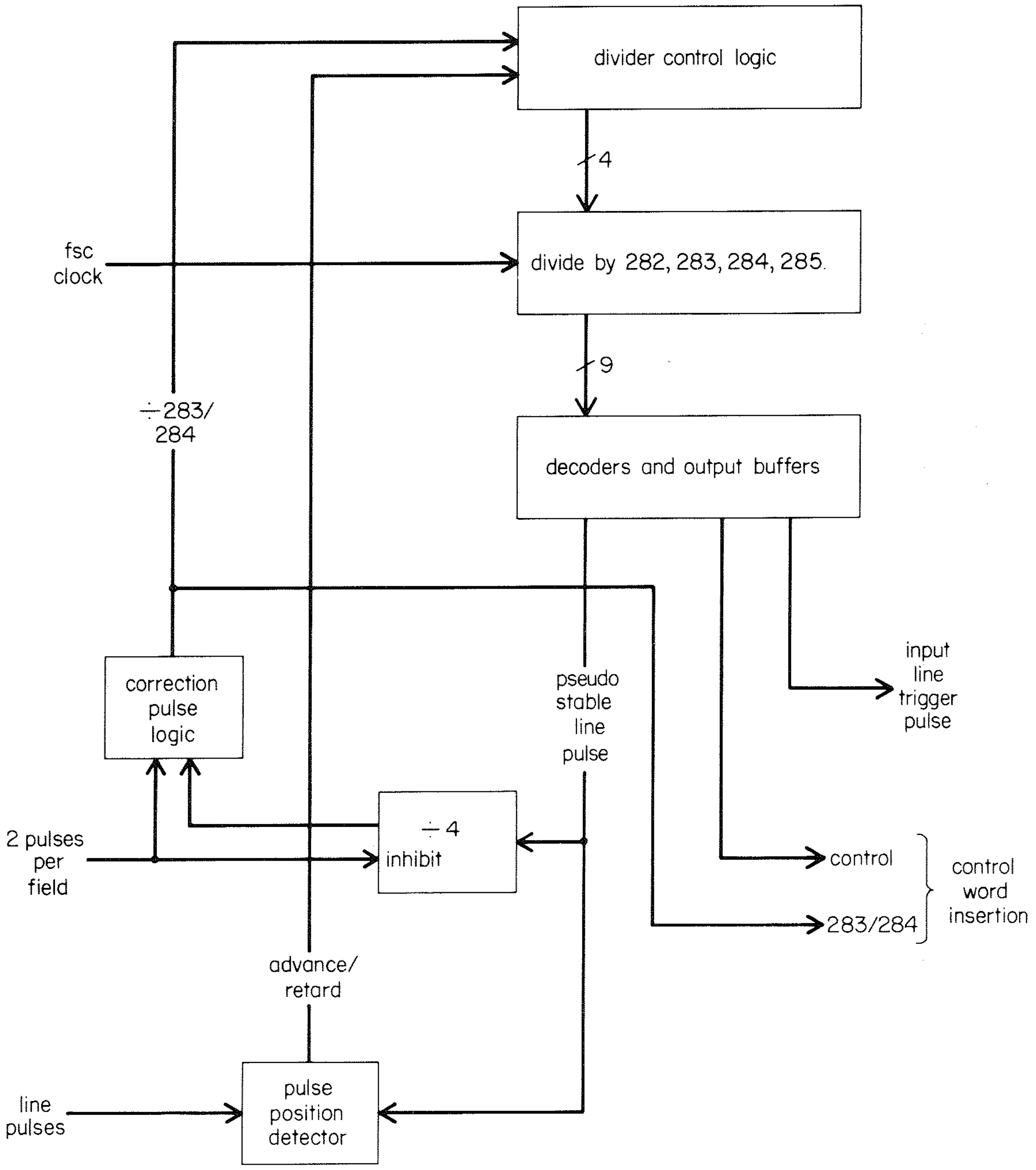

Fig. 6 - Block diagram of a line trigger generator

repetitive over this period of time. Many such sequences are possible, the one which gives the minimum variation from a 'truly' line-repetitive waveform being a complex sequence of division of the $3f_{sc}$ clock by 851 and 852. However, because the control logic operated at subcarrier frequency (1/3 clock rate) it was more convenient to have a sequence which alternated between two numbers which are both integer multiples of 3. Two such numbers are 849 and 852 (corresponding to division of the f_{sc} control system clock by 283 and 284). The data clock rate was exactly 851·2548 f_L, so that division by 852 for 3 lines followed by division by 849 for one line gave a division ratio of 851·25 — very nearly the correct ratio. The additional factor, 0·0048, was obtained by using two correction pulses per field, each of which interrupted this four-line sequence and caused an additional 'divide by 852', irrespective of what the four-line sequence would have done. The final sequence thus consisted of division by 852/849 according to the four-line sequence for 621 lines per picture plus four correction pulses of 852 per picture, giving a total of 625 lines. This sequence repeats every 4 pictures, or 8 fields. The correction pulses were derived from the line-rate store address counters and, for convenience, were applied outside the active picture area although, for minimum positional error, they ought to have been applied at equally spaced intervals.

The maximum deviation from uniformity of the line trigger position using this method of generation was ±3 clock pulses ($3f_{sc}$) and the stored line length had to be theoretically extended by 6 clock pulses to accommodate this variation. In practice this was not a serious problem as the commonly available types of storage conveniently give more storage per line than is required. The picture store, used in the experimental synchroniser, stores 768 samples per line whereas only 692 samples are required when the video is sampled at $3f_{sc}$.

After obtaining a pseudo line-repetitive pulse, it only remained to ensure that the mean position was correct relative to the pulses obtained from the line synchronising pulse separator. The pulse position detector had to have a window of at least ±3 clock pulses to accommodate the regular variation of line trigger pulse position, (in practice a total of 8 clock pulses wide), within which no phasing correction would occur. If the line synchronising pulse occurred outside this window, then the division ratio of the clock pulse counter was altered by ±1 depending on which side of the window it had occurred. This meant that the counter had to be variable over a range of ÷282 to ÷285 (that is, 283 ± 1, 284 ± 1). The detail design of this phasing circuit was additionally complicated by the requirement to behave predictably with non-mathematical input signals. During such inputs, a problem arises because the theoretically correct line frequency produced by the division ratio sequence is not equal to the actual input line frequency. The result of this frequency difference is that the line trigger pulse moves progressively to one end of the window. Phase corrections of 1 subcarrier period occur every time the error has built up to one subcarrier period.

Although a window of 8 clock pulses seems to be very wide and could lead to an uncertainty equivalent to 600 ns in the picture position, in practice, 6 clock pulses were taken up by the regular variation of the trigger pulse position. A further clock pulse was taken up by the inevitable uncertainty in the clocking of the line synchronising pulse, which left an effective window of 1 clock pulse which provided the necessary hysteresis for the system. Without the hysteresis, the phasing loop entered a limit cycle in which forward and reverse phase corrections occurred alternately.

In order that each line should be stored for the correct time interval it was essential that the data was read out from the store by an identical sequence of line trigger pulses, bearing exactly the same phase relationship, relative to the line numbers, as the input sequence. To achieve this object the output sequence was generated by an identical circuit. In addition, to obtain information at the output of the store about the phase of the sequence at the input, a control word was inserted into the data at the beginning of the line, before it was stored and subsequently extracted from the data at the store output. This control word represented the state of the input division ratio, excluding the phasing corrections, at the beginning of the active line and, after extraction from the output data, it was used to synchronise the output sequence counter.

Because the clocks driving the store control logic were directly locked to their respective subcarrier waveforms and the line trigger pulses were derived from these clocks, the output colour phasing was automatically achieved.

4.4. Store address counters

The write address counter was a simple binary counter, clocked by the input line trigger pulse and started by the input field pulse. At a time corresponding to the start of the active field, the store write process was enabled and the following 284 lines* of data were written into the store. The write-enable was then reset and the counter returned to the start number to await the next field pulse. The two decoded counter states used to control the write-enable bistable were also used as the correction pulses for the write line trigger pulse generator. (See Section 4.3).

A circuit was also included which assumed control of the counter on receipt of an input from the 'Non-Synchronous Cut Detector'. This circuit disabled the write-enable and reset the address counter immediately after a non-synchronous cut had been detected and it maintained the disabled state until the first field pulse of the 'new' input signal or for 10 ms whichever was the longer time. Thus, during this period, the store contents consisted of the last field received up to the cut, together with that part of the penultimate field which made up the space from the cut position to the end of the field. This information was available for use as a frozen field, to be displayed until the new signal had been stored and delayed long enough to bring it to the correct field phase. This arrangement results in a very short duration display of the frozen field, that is, a minimum of 10 ms and a maximum of 2½ field periods. The 10 ms was added to give a minimum time in which to allow the input circuits to lock to the new signal. A block diagram of the write address counter is given in Fig. 7.

The read address counter was basically similar to the write address counter but did not include the non-synchronous cut circuits. However, it did include a control system whose function was to modify the count according to the rules given in Table 2 (Section 3.2). The control system required inputs of the two quarter field-frequency ($F/4$) waveforms from the input synchronising pulse separator and the $F/4$ waveform from the output synchronising pulse separator. These three waveforms, together with the read field pulse, controlled the look-up table which advanced or delayed the start of the read address and read enable controls by one line as necessary. Fig. 8 shows a block diagram of the read address counter.

4.5. Non-synchronising cut detector

The non-synchronous cut detector was required to have a high probability of detecting genuine non-synchronous cuts and a very low probability of falsely indicating such a cut when none had occurred. It consisted of a counter and monostable combination which was used to generate an accurate window, centred on 64 μs from the previous line synchronising pulse edge. It responded only to line-to-line variations in the line period, because it was reset by every line synchronising pulse. Any variation

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* This is about 9 lines short of the full field but this was a limitation of the picture store in use.

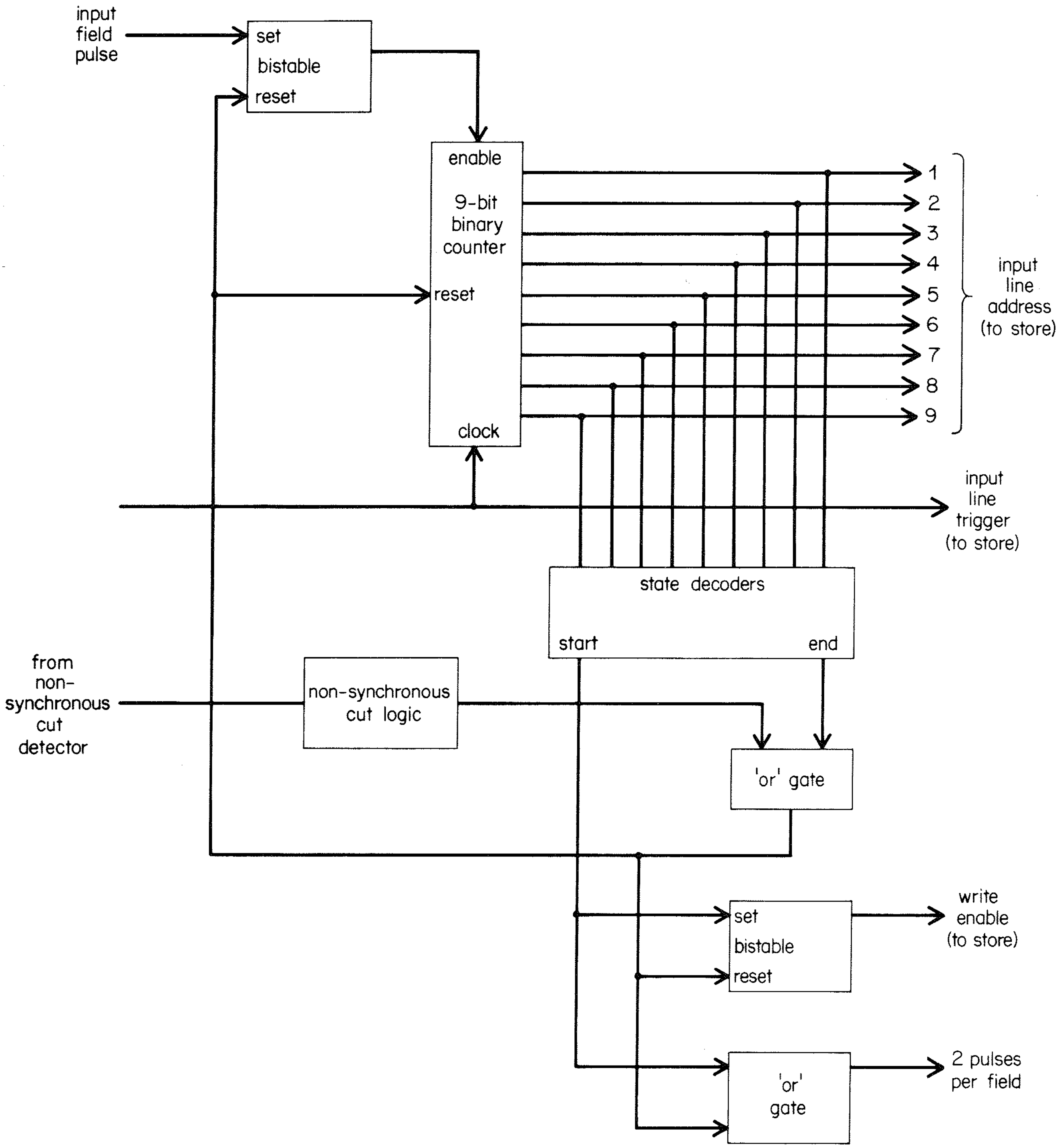

Fig. 7 - Block diagram of the input address counter

greater than a definite limit, or a complete cessation of line pulses initiated the 'non-sync cut' sequence of operations. The width of the timing window was variable, with a maximum value of 200 ns, centred on the mean pulse position.

4.6. Output processing

After the data has been read from the store, it was first digitally blanked in those parts which had not been stored, that is, for part of the line blanking and for the whole of the field blanking intervals. This was done prior to the d.a.c. in order to remove spurious 'end-effects' generated by the store. This process provided a clean, uniform signal level which, after the d.a.c., was blanked to remove the input burst. New synchronising pulses and burst were derived from the output reference signals and inserted into the output video waveform.

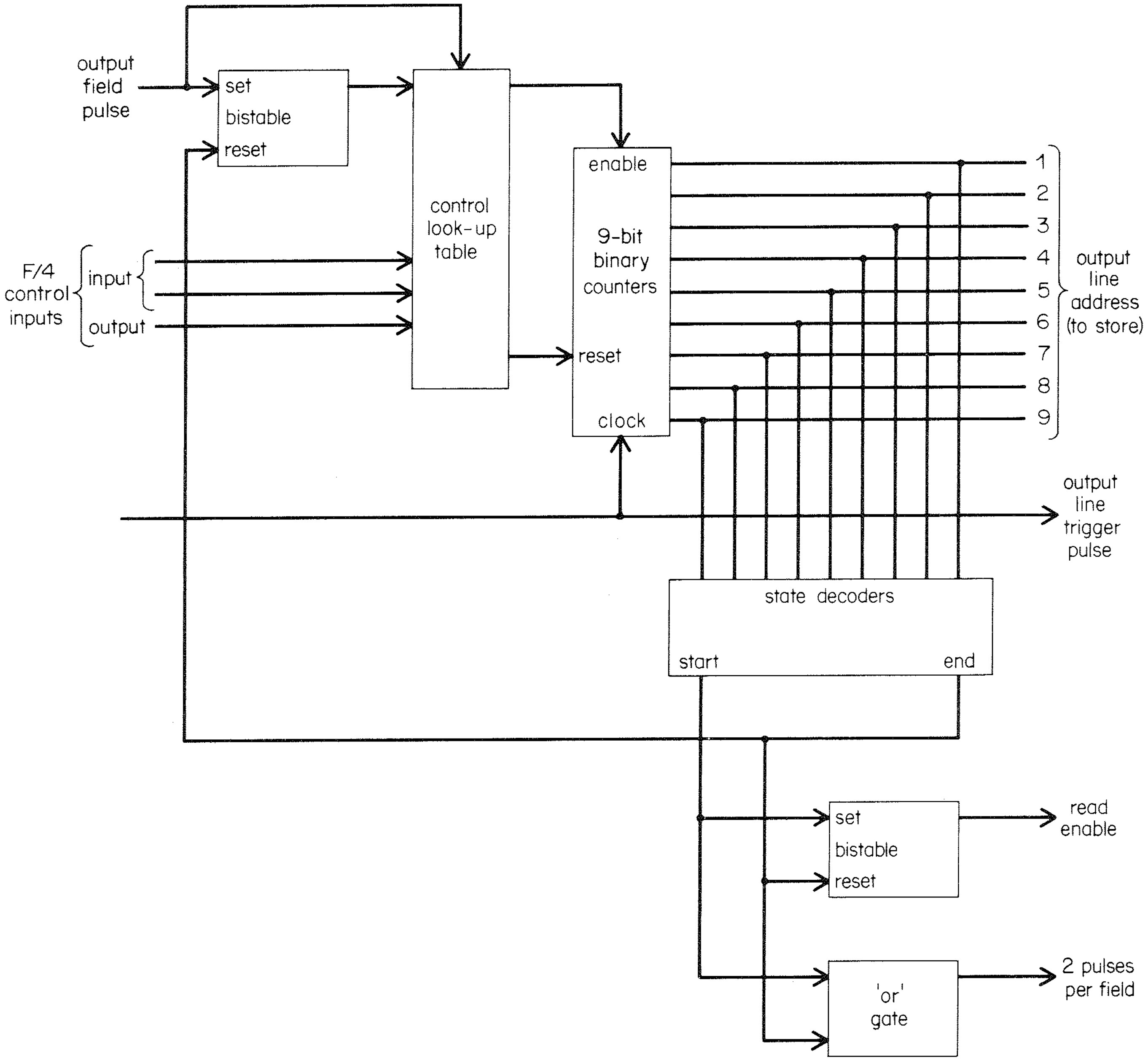

Fig. 8 - Block diagram of the output address counter

5. Performance of the simple synchroniser

Apart from a number of detail problems, the overall performance of the experimental prototype was satisfactory. It appeared that the basic philosophy was correct and that most of the circuits which had been developed were basically adequate, although tests showed that some required slight instrumental modifications.

Appendix 1 gives some test results obtained by attenuating the appropriate waveforms. While reduced amplitude signals would not normally be expected in the position occupied by a synchroniser in the network, these results give a measure of the margins available.

Some problems were encountered and some deficiencies identified during tests and demonstrations. These could be broadly divided into two groups. The first group consisted of those difficulties which were associated with the use of the Research Department 1975 picture store. These were: (a) improper operation when the input and output signals were within 4 lines of field synchronism or when the line phase difference was nearer than about ±100 ns to a certain critical value; (b) the frozen field, produced just after a non-synchronous cut, contained a band of mid-grey level signal lasting for about 4 field lines at the point where the cut occurred. Problem (a) would be completely overcome by the user of a new field store, specifically designed for use in a synchroniser. Problem (b) cannot be totally overcome with only one field of storage as there is inevitably some vertical discontinuity in the picture. It is possible, however, that this effect could be very much reduced by arranging the store addresses in such a way that the store always contains rather more than one complete field of information at all times. Because all of these problems were related to the store and new solutions would have to be developed for a new store, nothing was done about them at this experimental stage of the work.

The second group of problems consisted of the choice of clock frequency (see Section 3.3 and Appendix 2) and a number of details associated with the individual circuit blocks which will be discussed under the same headings as in Section 4.

5.1. Synchronising pulse separators

The input synchronising pulse separator was satisfactory in all respects except for the way in which it derived the input PAL square wave. This was done by detecting the first burst of each field and assuming that it corresponded to the positive sense of the V-axis switch, that is, the $R-Y$ signal non-inverted. This first burst was used to check that the half line-frequency bistable was in the correct phase and to reset it if it was not. With signals which conform to the PAL specification,[2] this is a perfectly satisfactory way of carrying out this function, but it was noticed that, on one occasion, the input signal did not so conform and the output picture was produced with the wrong phase of V-axis switch. Although, on that occasion, it was the input signal which was incorrect, nevertheless, this constituted an avoidable weakness in the design. An alternative method of deriving the PAL switch phase is the more conventional one of amplifying and filtering the 7·8125 kHz component from the output of the burst phase detector. In view of the proposed modifications to the non-synchronous cut detector (Section 5.5) this alteration is necessary in any case.

The output synchronising pulse separator was judged to be completely satisfactory.

5.2. Clock oscillators

The input clock oscillator was only marginally acceptable in its lock-up time after non-synchronous cuts – it could take as long as 60 ms before being within a reasonable error-band of its long term specification. In all other respects, it was satisfactory. However, it is not proposed to use this circuit in further work on synchronisation as there already exists a completely digital (except for the actual oscillator) phase-lock loop whose overall performance is adequate and which has a shorter lock-up time. This digital loop controls the sampling phase by using the data output from the a.d.c. Thus, the entire input clock system could be contained within a feedback loop and all manual controls on the input circuit, in particular the delay between the clock oscillator and the a.d.c. could be eliminated. This loop would also provide a 1/3 clock frequency waveform and a continuously derived PAL square wave for use in other parts of the synchroniser.

The output clock generator was completely satisfactory, indeed Appendix 1 shows that the reference subcarrier input could be attenuated by 30 dB before very noticeable picture impairment occurred and then only if a simple PAL decoder was used.

5.3. Line trigger generators

The line trigger generators worked satisfactorily except that during the critical period near line synchronism, a store malfunction caused the control word to be shifted. The resulting loss of control caused most of the effects visible on the output picture during this critical period.

The input and output line trigger generators were fundamentally identical. Therefore, the performance of the synchroniser with non-mathematical signals was the same whether the non-mathematicality was of the input signal or of the output reference pulses.

5.4. Store address counters

The only problem encountered with the store address counters was the method of driving the control look-up table for the output counter. As designed, the control waveforms were only verified every 4 fields. This resulted in a delay of up to 4 fields before the V-axis switch was corrected after a non-synchronous cut. A modification to verify those waveforms at the beginning of every output field would virtually eliminate this problem in all but the worst-case combination of input, output and cut timings.

5.5. Non-synchronous cut detector

The design philosophy of the non-synchronous cut detector, which consisted of looking for line-to-line variations of line length, was found to be inadequate. Because of the amounts of pulse jitter encountered in practice, the detector window must be increased from 200 ns to about 600 ns in order virtually to eliminate false triggering. This would mean that approximately 1% (600 ns ÷ 64 μs) of all non-synchronous cuts would not be detected until the occurrence of an input field pulse either earlier or later than expected. The consequence of this on the output picture would be that the last output field would consist partly of the 'old' signal and partly of information from the 'new' signal, the latter being randomly positioned both horizontally and vertically. This output would remain 'frozen' for ½ to 2½ field periods, until the input circuits had locked to the new signal. The visual effect of this is very disturbing and it could also result in spurious line and field synchronising pulses in the active picture area. By adding inputs of V-axis switch and burst-phase continuities to the detector, the proportion of such cuts could be reduced. If the burst phase continuity detector was to have a window of $\pm 30^\circ$, then the addition of these two inputs would reduce the incidence of missed cuts to 1 in 1200, $((1/100) \times \frac{1}{2} \times (60/360))$.

5.6. Output processing

The blanking, synchronising pulse and burst reinsertion circuits were adequate for experimental work but it is likely that they could be replaced by standard units with better performance, particularly with better differential gain and phase characteristics, in any further development of this work.

6. Further work

The next stage in this work would be the design and construction of a prototype synchroniser for use in extensive field trials. This would involve the design of a new store, specifically configured to operate as a synchroniser, thus eliminating the problems associated with the use of the Research Department 1975 picture store. Such a store would be very much smaller, and would probably need only 4 x 4U standard cards from the BBC BMM range.

Apart from the detail problems already dealt with, the only other outstanding problem is the processing of monochrome signals. For monochrome operation, the clocks would have to be locked to the line pulse in some way as no burst would be available. It is proposed that the same oscillators be used but locked to the line-synchronising pulses using the pseudo-stable line trigger pulses. If the two correction pulses per field were disabled, then the lowest spurious frequency present in the line phase detector output would be ¼-line rate or about 3·9 kHz. It should not prove too difficult to filter out such a frequency. The resultant clock frequency would be only 5 parts in 10^6 different from the colour locked case. This difference should be easily accommodated by the oscillators.

Monochrome operation requires the inclusion of a burst detector to switch off the two correction pulses per field, to switch over the phase detectors and loop filters, to disable the read address control look-up table and to inhibit the insertion of the output burst. The timing stability of the resulting synchroniser would be considerably less than for colour operation, but monochrome processing does not require the same degree of stability because of the absence of the colour subcarrier.

7. Conclusions

This work demonstrated the feasibility of a simple digital synchroniser using only one field of storage, suitable for network operations as an alternative to the Natlock system used at present. It achieved its objective of identifying the problems which would be encountered in designing a field-trials prototype machine, and their likely solutions.

As a study of the synchronising problems encountered during network operations it has provided a basis on which to design equipment to overcome these problems.

8. References

1. WALKER, R. *and* McNALLY, G.W.W. An experimental digital picture store. BBC Research Department Report No. 1977/9.

2. Specification of television standards for 625-line System I transmissions. ITA and BBC, January 1971.

9. Appendix 1

Test results obtained by attenuating the inputs.

Input	Attenuation dB	Remarks
Input signal (colour bars)	11·0	Input clock oscillator just locks in from no-signal condition.
	12·0	Input clock oscillator just locks in on non-synchronous cuts.
		Output occasionally has wrong phase of V-axis switch, and some horizontal instability.
	12·5	Output freezes. This level of input signal is regarded as no input.
Reference Mixed Synchronising Pulses	29	Output picture disappears.
Reference Burst Gate	29	Output burst reduced to half normal duration.
	29·5	Output burst disappears.
Reference Mixed Blanking	11·5	Input burst breaks through on output.
Reference Subcarrier	30	Colour phase errors occur.

10. Appendix 2

Choice of clock frequency:— Results.

The experimental prototype was originally designed using line-locked clocks (851 f_L). Tests showed that, even with the output phase detector, the short-term colour subcarrier phase errors could not be reduced to less than about 10° – 20°, peak to peak. Two factors which were thought to be jointly responsible for this phase jitter were the input synchronising pulse jitter and the relatively small amount of timing information contained within a single line pulse edge. Measured values of pulse jitter varied from better than 20 ns to worse than 140 ns peak to peak with large components at the field rate (50 Hz). This made the design of the phase lock loops for the clock generators very difficult, and even with loop bandwidths of the order of 1–2 Hz, significant amounts of phase modulation occurred. Such loops were made complicated by the additional requirement for rapid lock-up to a new input signal. This required an in-lock detector which altered the effective bandwidth of the loop depending on whether it was in-lock or not.

The small amount of timing information contained in a single pulse edge made the loops very sensitive to noise at the input to the slicing circuit, resulting in a very poor effective input noise bandwidth. With the slicing circuit used initially, noise inputs up to 50 MHz would perturb the position of the output pulse. This is a similar problem to that which occurs in sampled data systems in which the sampling process can 'mix-down' high frequency noise into the baseband.

The output phase detector, which used the stored input burst as a timing reference for the output, should have reduced the output jitter. But, in order to correct for the errors introduced by the input loop, it was required to have a bandwidth much greater than the input loop. In fact, it reduced the phase errors by nearly two orders of magnitude but this was still inadequate. In addition, such an output clock system cannot operate until the signal is being output from the store. This sometimes introduced an unacceptable delay in obtaining the correct colour phase and some horizontal picture instability after a non-synchronous cut.

Changing to subcarrier-locked clocks gave an immediate improvement in stability as a result of the fundamental stability of the colour subcarrier and the better effective input signal to noise ratio. A burst phase detector averages the signal over a 2 μs period, resulting in an equivalent input noise bandwidth of 500 kHz. This is an improvement over the line locked oscillator of roughly two orders of magnitude, equivalent to a 20 dB reduction in the noise power. Even if the slicing circuit of the line locked clock phase detector is preceded by an ideal 5 MHz low pass filter, the colour locked system still has a ten-fold advantage.

As well as having the advantage of smaller output jitter, using subcarrier locked clocks enabled the colour-locking of the output to be made a function of the clocks and the store control logic so that the output phase detector and its associated delay could be eliminated. The cost of this change was a small increase in the complexity of the control logic.

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